**In the Claims**

Please amend Claims 1-5, 7-8, delete Claims 6, 9-23, and add Claims 24-52 as follows:

1. (Previously Amended) A system for enabling device communication in an expanded computing device comprising:

a primary bus coupled to a first integrated circuit ~~chip~~ having a first register and a second register therein;

a secondary bus physically remote from the primary bus coupled to a second integrated circuit ~~chip~~ having a third register and a fourth register therein;

a first serial link coupled between the first register and the third register; ~~and~~

a second serial link coupled between the second register and the fourth register.; and

wherein the first integrated circuit is configured to enable the transfer of data to the second integrated circuit without using caching.

2. (Previously Amended) The system of claim 1 wherein the first integrated circuit ~~chip~~ is an application specific integrated circuit (ASIC) ~~chip~~.

3. (Previously Amended) The system of claim ~~2~~ 7 wherein said first interface is adapted to send a tag to the second interface indicative of a bus transaction type ~~wherein the first integrated chip is configured to enable the transfer of data to the second integrated chip without using caching~~.

4. (Previously Amended) The system of claim ~~2~~ 1 wherein the second integrated circuit ~~chip~~ is adapted ~~configured~~ to ~~enable the~~ transfer ~~of~~ data to the first integrated circuit ~~chip~~ without using caching.

5. (Previously Amended) ~~The system of claim 1 further comprising a primary bus coupled to the first integrated chip.~~

An interface, comprising:

an interface adapted to interface parallel data from a parallel data bus to a first bus; and

a module adapted to interface the parallel data from the parallel data bus into serial data adapted to interface with a second remote bus, the module converting the parallel data to the serial data without using caching.

6. (Delete) ~~The system of claim 1 further comprising a secondary bus coupled to the second integrated chip.~~

7. (Previously Amended) The system of claim ~~5~~ 1 further comprising a first interface coupled between the primary bus and the first register and the second register, the first interface configured to determine if a pending address provided thereto represents a transaction to be communicated to the second integrated circuit.

8. (Previously amended) The system of claim ~~6~~ 7 further comprising a second interface coupled between the secondary bus and the third register and the fourth register.

9-23. Delete

24. (New) An interface, comprising:

a circuit adapted to couple to a first bus having parallel bus data, the circuit adapted to serially send the bus data over a link to a physically remote second bus without requiring or waiting for an incoming acknowledgement over the link before inaugurating a transfer of the serialized bus data over the link.

25. (New) The bridge according to claim 24 wherein the first bus is a PCI-type bus.

26. (New) The bridge according to claim 24 wherein the circuit is an integrated circuit.

27. (New) The bridge according to claim 26 wherein the integrated circuit is an application specific integrated circuit (ASIC).

28. (New) The bridge according to claim 24 wherein the circuit is operable to exchange bus data according to a predetermined hierarchy giving the first bus a higher level than the second bus.

29. (New) The bridge according to claim 24 further comprising a first register adapted to hold parallel bus data.

30. (New) The bridge according to Claim 29 further comprising a second register adapted to hold received second bus data.

31. (New) A bridge accessible by a processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, said bridge comprising:

a link;

a first interface coupled between said first bus and said link; and

a second interface adapted to couple between said second bus and said link, said first interface and said second interface being operable to transfer bus data serially through said link without waiting for an incoming acknowledgment over said link before inaugurating a transfer of said bus information over said link.

32. (New) The bridge according to claim 31 wherein said first interface and said second interface are operable to exchange information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus.

33. (New) The bridge according to claim 31 wherein said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface being operable in response to a pending transaction on said first bus to begin processing said pending transaction and to apply a retry signal to at least one of said signaling lines of said first bus before the pending transaction on said first bus has been transmitted to and acknowledged by said second bus.

34. (New) The bridge according to claim 33 wherein less than all of the information on the signaling lines of said first bus is transmitted by said first interface over said link.

35. (New) The bridge according to claim 31 wherein said first interface is selectively responsive to those addresses appearing on said first bus that are on a predetermined schedule of addresses corresponding to the bus-compatible devices accessible through said second bus, in order to avoid responding to addresses corresponding to other ones of the bus-compatible devices on said first bus.

36. (New) The bridge according to claim 35 comprising:

a register for storing said predetermined schedule.

37. (New) The bridge according to claim 35 wherein said first interface comprises:

a first register for storing said predetermined schedule, said second interface comprising:

a second register for storing said predetermined schedule.

38. (New) The bridge according to claim 36 wherein said register is operable to establish with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus.

39. (New) The bridge according to claim 31 comprising:

a register for establishing with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus.

40. (New) The bridge according to claim 31 wherein said first interface and said secondary interface are operable to permit communication between bus-compatible devices on said second bus without routing through said first bus.

41. (New) The bridge according to claim 31 wherein said first interface and said second interface comprise:

a first and a second programmable logic device connected between said link and said first bus and said second bus, respectively.

42. (New) The bridge according to claim 31 wherein said first interface and said second interface comprise:

a first and a second application-specific integrated circuit connected between said link and said first bus and said second bus, respectively.

43. (New) The bridge according to claim 42 wherein said first and said second application-specific integrated circuit are identically structured and each have a control pin for receiving a control signal to establish operation in one of two modes.

44. (New) The bridge according to claim 42 wherein said first and said second application-specific integrated circuit each comprise:

a plurality of ports coupled to said second interface for providing input/output.

45. (New) The bridge according to claim 31 wherein said processor is interrupt-driven, said second interface being operable to transmit through said link to said first interface interrupt signals destined to interrupt the processor.

46. (New) The bridge according to claim 45 wherein said processor is responsive to error signals, said second interface being operable to transmit through said link to said first interface error signals destined to affect the processor.

47. (New) The bridge according to claim 31 wherein said first bus operates at a predetermined clock speed, said link being operable to propagate data between said first interface and said second interface at a bit transfer rate greater than said predetermined clock speed.

48. (New) The bridge according to claim 47 wherein said link comprises:

a pair of simplex links for sending information in opposite directions.

49. (New) The bridge according to claim 48 wherein said simplex links are driven for differential signal transfers.

50. (New) The bridge according to claim 31 wherein said second bus comprises a PCI bus.

51. (New) The bridge according to claim 31 wherein said second interface is operable in response to a transaction from said link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus-compatible devices on said second bus for transmission back over said link in order to satisfy pending and anticipated transactions.

52. (New) The bridge according to claim 31 wherein said first interface and said second interface are operable to permit at least one of the bus-compatible devices on said second bus to address one or more of the bus-compatible devices on said first bus using on said second bus substantially the same type of addressing as is used to access devices on said second bus.